WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

a first insulating film formed over said semiconductor substrate;

a second insulating film formed on said first insulating film;

a contact plug made of a conductive material, said plug vertically penetrating said first and second insulating films and extending on said second insulating film; and

a conductive film in contact with the upper surface of said contact plug and part of said second insulating film.

2. A device according to claim 1, wherein said first and second insulating films are transparent in relation to visible light.

3. A semiconductor device comprising:

a semiconductor substrate having a memory cell region and a peripheral region;

an alignment mark for positioning which is made of a conductive material and formed in said peripheral region;

a first insulating film which covers said alignment mark and extends to said memory cell region;

a second insulating film formed on said first insulating film;

a contact plug made of a conductive material, said plug vertically penetrating said first and second

insulating films and extending on said second insulating film;

a storage node in contact with the upper surface of said contact plug and part of said second insulating film; and

a dielectric film which covers said storage node and is in contact with said second insulating film.

4. A device according to claim 3, wherein said first and second insulating films are transparent in relation to visible light.

5. A device according to claim 1, wherein said first insulating film is a silicon oxide film, and said second insulating film is a silicon nitride film which grew through a low-pressure chemical vapor deposition process.

6. A device according to claim 3, wherein said first insulating film is a silicon oxide film, and said second insulating film is a silicon nitride film which grew through a low-pressure chemical vapor deposition process.

7. A method of manufacturing a semiconductor device, comprising the steps of:

forming a first insulating film above a semiconductor substrate;

forming a second insulating film on said first insulating film;

forming a third insulating film on said second insulating film, said third insulating film having a low

etching rate in relation to a first etchant for said first insulating film;

forming an opening portion so as to extend through said third and second insulating films up to said first insulating film;

forming a spacer on the side wall of said opening portion, said spacer having a low etching rate in relation to said first etchant for said first insulating film;

forming a contact hole so as to extend through said first insulating film, using said third insulating film and said spacer as masks;

filling said opening portion and said contact hole with a first conductive material to form a contact plug; and

selectively removing said third insulating film using a second etchant whose etching rate to said second insulating film is low.

8. A method according to claim 7, further comprising, after the step of selectively removing said third insulating film, the steps of:

forming a fourth insulating film so as to cover the exposed surfaces of said contact plug and said spacer;

forming a second contact hole in said fourth insulating film so as to expose part of the surface of said contact plug and at least part of the side surface of said spacer;

forming a second conductive material on the side and

bottom surfaces of said second contact hole;

selectively removing said fourth insulating film using an etchant whose etching rate to said second conductive material and said second insulating film is low.

9. A method according to claim 8, wherein said second conductive material is used as a storage node of DRAM.

10. A method according to claim 7, wherein said first, second, and third insulating films are transparent in relation to visible light.

11. A method according to claim 10, wherein said first insulating film is a silicon oxide film, said second insulating film is a silicon nitride film which grew through a low-pressure chemical vapor deposition process, and said third insulating film is a silicon nitride film which grew through a plasma chemical vapor deposition process.

12. A method according to claim 11, wherein said silicon nitride film which grew through said plasma chemical vapor deposition process, is removed with an aqueous solution of hydrofluoric acid, using, as an etching stopper, said silicon nitride film which grew through said low-pressure chemical vapor deposition process.

13. A method according to claim 11, wherein the thickness of said silicon nitride film which grew through said plasma chemical vapor deposition process, is eight

times or less that of said silicon nitride film which grew through said low-pressure chemical vapor deposition process.

14. A method of manufacturing a semiconductor device having a memory cell region and a peripheral region, comprising the steps of:

forming an alignment mark for positioning made of a conductive material, in said peripheral region;

forming a first insulating film so as to cover said alignment mark and extend to said memory cell region;

forming a second insulating film on said first insulating film;

forming a third insulating film on said second insulating film, said third insulating film having a low etching rate in relation to a first etchant for said first insulating film;

forming an opening portion so as to extend through said third and second insulating films up to said first insulating film;

forming a spacer on the side wall of said opening portion, said spacer having a low etching rate in relation to said first etchant for said first insulating film;

forming a first contact hole so as to extend through said first insulating film, using said third insulating film and said spacer as masks;

filling said opening portion and said first contact hole with a first conductive material to form a contact

plug; and

selectively removing said third insulating film using a second etchant whose etching rate to said second insulating film is low.

15. A method according to claim 14, wherein said first, second, and third insulating films are transparent in relation to visible light.

16. A method according to claim 15, wherein said first insulating film is a silicon oxide film, said second insulating film is a silicon nitride film which grew through a low-pressure chemical vapor deposition process, and said third insulating film is a silicon nitride film which grew through a plasma chemical vapor deposition process.

17. A method according to claim 16, wherein said silicon nitride film which grew through said plasma chemical vapor deposition process, is removed with an aqueous solution of hydrofluoric acid, using, as an etching stopper, said silicon nitride film which grew through said low-pressure chemical vapor deposition process.

18. A method according to claim 16, wherein the thickness of said silicon nitride film which grew through said plasma chemical vapor deposition process, is eight times or less that of said silicon nitride film which grew through said low-pressure chemical vapor deposition process.

19. A method according to claim 14, further

comprising, after the step of selectively removing said third insulating film, the steps of:

forming a fourth insulating film so as to cover the exposed surfaces of said contact plug and said spacer;

forming a second contact hole in said fourth insulating film so as to expose part of the surface of said contact plug and at least part of the side surface of said spacer;

forming a second conductive material on the side and bottom surfaces of said second contact hole;

selectively removing said fourth insulating film using an etchant whose etching rate to said second conductive material and said second insulating film is low.

20. A method according to claim 19, wherein said spacer is made of a conductive material and electrically connected to said second conductive material together with said contact plug.

21. A method according to claim 19, wherein said second conductive material is used as a storage node of DRAM.